Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-20 (Canceled):

Claim 21 (Currently Amended): A semiconductor device having an access time measuring test mode, comprising:

a circuit block to which an input signal is input at a timing in accordance with an input clock, and which outputs an output signal having a value corresponding to said input signal;

a first signal path for guiding a test input signal, which has been supplied to a first pad, to a signal input terminal of said circuit block;

a second signal path for guiding a test clock, which has been supplied to a second pad, to a clock input terminal of said circuit block;

a third signal path for guiding a test output signal, which has been output from a signal output terminal of said circuit block, to a third pad; and

a fourth signal path for guiding said test clock, which is input to said clock input terminal, to a fourth pad,

wherein said third and fourth signal paths are formed so that wiring delay time of said third and fourth signal paths are substantially equal,

wherein said fourth signal path comprises a selector, responsive to a mode of a selection signal, that selectively supplies a prescribed signal or said test clock directly to said fourth pad, and

wherein said fourth signal path does not include a delay circuit.

Claim 22 (Currently Amended): The semiconductor device according to claim 21, wherein said first signal path comprises a second selector which during a normal operation supplies an output signal from a preceding circuit block to said signal input terminal of said circuit block, and which during a test operation supplies said test input signal to said signal input terminal of said circuit block.

Claim 23 (Currently Amended): The semiconductor device according to claim 21, wherein said second signal path comprises a second selector which during a normal operation supplies a normal clock to said clock input terminal of said circuit block, and which during a test operation supplies said test clock to said clock input terminal of said circuit block.

Claim 24 (Currently Amended): The semiconductor device according to claim 21, wherein said third signal path comprises a second selector which during a normal

operation supplies a prescribed signal other than said test output signal to said third pad, and which during a test operation supplies said test output signal to said third pad.

Claims 25-42 (Canceled)